AMENDMENTS TO THE CLAIMS:

Claims 1-12. (cancelled):

13.(original) A delay locked loop circuit for maintaining phase synchronization between a received spreading code included in a spread-spectrum signal and a reference spreading code, comprising:

a reference spreading code generator for generating the reference spreading code;

a combined code generator for generating a combined spread code from the reference spreading code;

arithmetic means for detecting a phase difference between the received spread code and the reference spread code using the combined spreading code; and

voltage controlled oscillator for controlling a phase of the reference spreading code on the basis of the phase difference.

14.(original) The delay locked loop circuit of claim 13, wherein the arithmetic means includes a multiplier for multiplying the received spreading code by the combined spreading code, and filter for filtering an output of the multiplier.

15.(original) The delay locked loop circuit of claim 13, wherein the combined code generates first weights and then combines a plurality of phase shifted occurrences of the reference spreading code.

16.(original) The delay locked loop circuit of claim 15, wherein the combined code generator makes positive, and successively reduces in magnitude, the weights of n-number of

reference spreading codes of small phase shift constituting a first half of 2n- (where n is a positive integer) number of reference spreading codes that have been successively shifted in phase, and makes negative, and successively increases in magnitude, the weights of n-number of reference spreading codes of large phase shift constituting a second half of the reference spreading codes that have been successively shifted in phase.

17.(original) The delay locked loop circuit of claim 16, wherein a plurality of weights for which the n is different, outputting the combined spreading code using a weight for which n is large, and outputting a combined spreading code using the weight for which n is small whenever the phase difference falls below a set value.